

Notice of References Cited

Application/Control No.

09/434,736

Applicant(s)/Patent Under
Reexamination
KIM ET AL.

Examiner

Evan T. Pert

Art Unit

2829

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-5,683,938	11-1997	Kim et al.	438/640
	B	US-5,162,261	11-1992	Fuller et al.	438/640
X	C	US-5,069,749	12-1991	Gutierrez, Jean-Marie	427/124
	D	US-4,917,759	04-1990	Fisher et al.	204/192.35
	E	US-5,366,848	11-1994	Thane et al.	216/47
	F	US-5,320,981	06-1994	Blalock, Guy T.	438/640
X	G	US-4,999,318	03-1991	Takahumi et al.	204/192.34
	H	US-4,495,220	01-1985	Wolf et al.	204/192.37
	I	US-4,902,377	02-1990	Berglund et al.	204/192.36
	J	US-4,369,090	01-1983	Wilson et al.	216/48
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lee et al., "Chemical Vapor Deposition of Tungsten (CVD W) as Submicron Interconnection and Via Stud", J. Electrochem. Soc., Vol. 136, No. 7, July 1989, pages 2108-2112.
	V	Saia et al., "Plasma Etching Methods for the Formation of Planarized Tungsten Plugs Used in Multilevel VLSI Metallizations", J. Electrochem. Soc.: Solid State Science and Technology, Vol. 135, No. 4, April 1988, pages 936-940.
	W	Wolf, SILICON PROCESSING FOR THE VLSI ERA VOLUME 2: Process Integration, 1986, Lattice Press, page 106.
X	X	Wolf, SILICON PROCESSING FOR THE VLSI ERA VOLUME 2: PROCESS INTEGRATION, 1990, Lattice Press, Chapter 4, pages 176-297.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.